

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): PARENT et al.

Serial No.: 10/799,742

Group Art Unit: 2827

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Filed: March 12, 2004

Examiner: Mai, Son Luu

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Title: Method and Circuit for Reducing
Defect Current From Array Element
Failures in Random Access Memories

Attorney Docket No.: CD03011

**AMENDMENT AFTER FINAL ACTION
(37 C.F.R. §1.116)**

5 Mail Stop AF
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

10 A. Introductory Comments

The following is submitted in response to the FINAL Office Action dated October 31, 2005 and is currently due February 28, 2006, with a one month extension.

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37 C.F.R. 61.8

I hereby certify that this correspondence is being

30 transmitted via facsimile to the United States Patent and Trademark Office to fax number: 1-571-273-8300
 Date of Transmittal: FEBRUARY 28, 2006[] deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents,
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Typed/Printed Name: Bradley T. Sako40 Signature: BradyEntry is approved
03/11/06